IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

SYNOPSYS, INC., a Delaware Corporation, Plaintiff and Counter-Defendant, v. MAGMA DESIGN AUTOMATION, a Delaware Corporation, Defendant and Counterclaimant. AND RELATED COUNTERCLAIMS.	C.A. No. 05-701 GMS

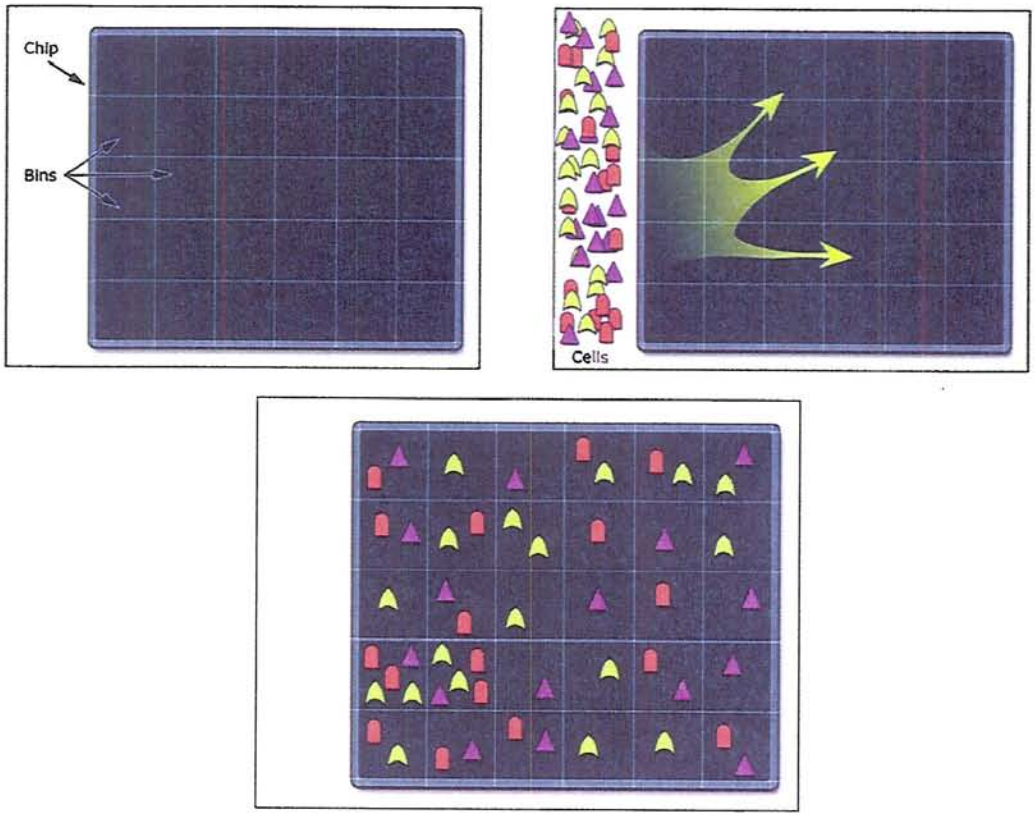
DECLARATION OF EDMOND S. COOLEY, D. Eng.

I, Edmond S. Cooley, have personal knowledge of all the facts and opinions contained herein and, if called to testify, could and would competently testify thereto.

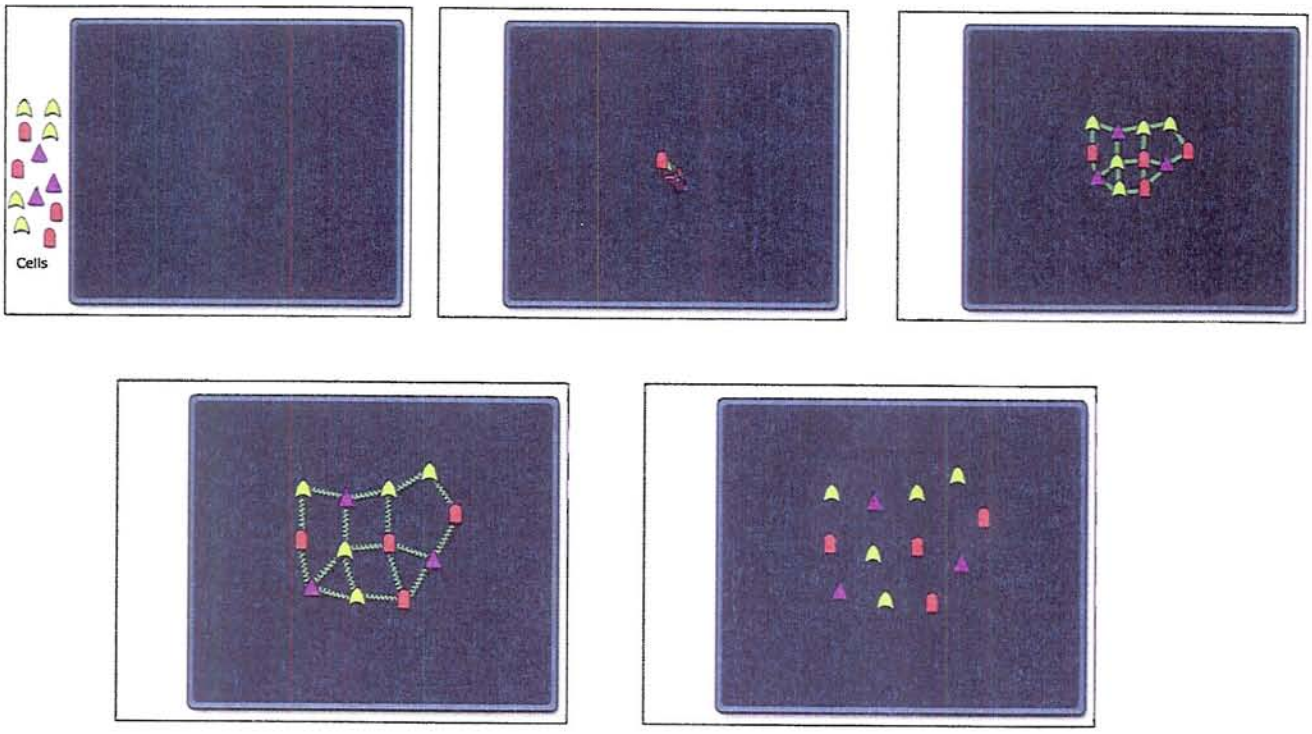
1. My education, credentials, and work experience are described in my previously provided declaration dated November 3, 2006.

2. I have reviewed the '508 patent, its prosecution history, "Plaintiff Synopsys, Inc.'s Opening Claim Construction Brief" and the "Declaration of David Harris, Ph.D. in Support of Synopsys, Inc.'s Opening Claim Construction Brief."

3. Partition-based placement techniques such as Min-Cut placement, which were commonly used in 1998, have, in practice, been almost entirely replaced with the Force-Directed technique introduced in the proceedings of DAC in June 1998. Partition-based placement techniques used bins, as illustrated below:



4. The Force-Directed technique places cells in one location on a chip and then simulates the connections between those cells as springs. The cells are moved in response to the attractive and repulsive forces exerted by the springs for any particular placement of the cells. With successive iterations, improved placements of the cells are typically identified and an optimal placement can be approximated. The Force-Directed technique is illustrated as follows:



5. The '508 patent discloses two ways to relieve congestion (1) a one step process using logic modifications that directly relieve congestion by for example, reducing the number of pins, and (2) a two-step process of performing logic modifications to create some timing slack, and then moving the cells to relieve congestion. In the two-step process, the first step is a precursor to the congestion-improving step. This two-step process is illustrated with reference to the figures below.

Figure 1

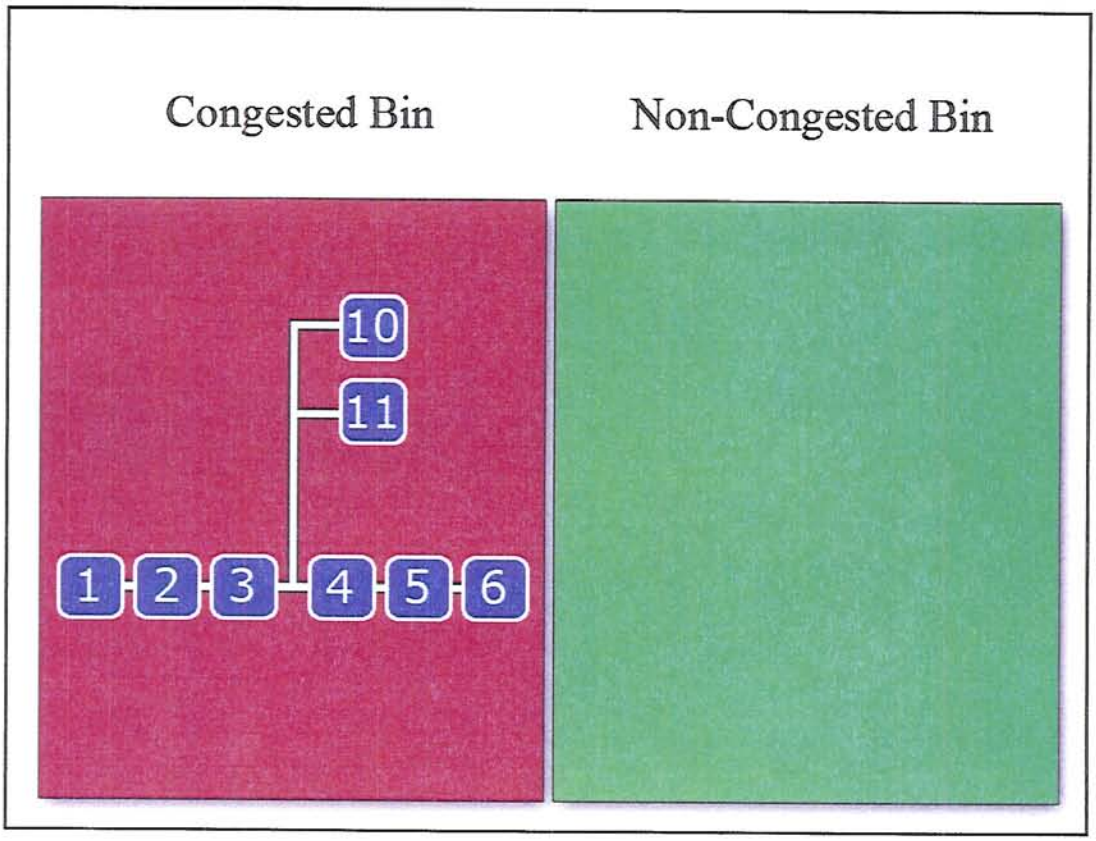


Fig. 1 shows two bins on a chip, with cells 1-6 placed close together for timing purposes in one of the bins. The short wires between the cells help the circuit operate faster – but the large number of cells in that bin creates congestion.

Figure 2

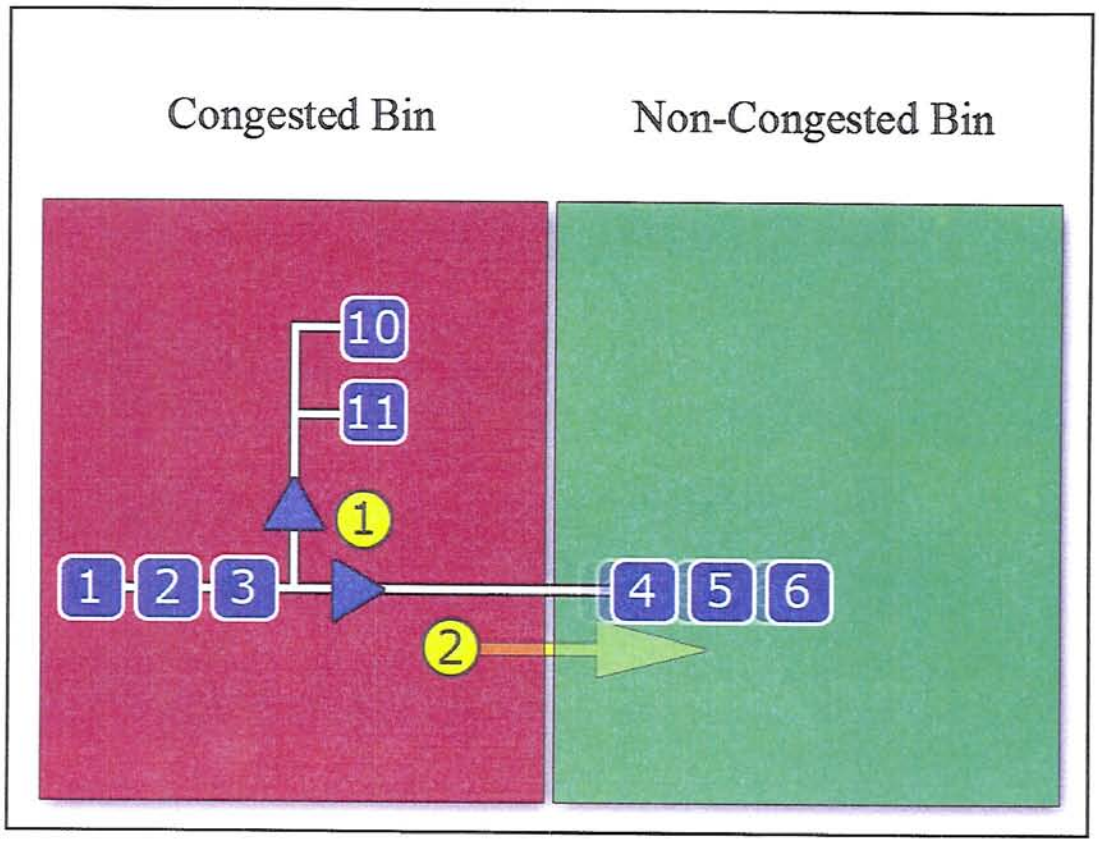


Fig. 2 illustrates the two-step process. If the connection between cells 3 and 4 can be made faster, for example, with the addition of two triangular shaped buffers shown as step 1, the wires between cells can be longer and cells 4-6 can be moved to the non-congested bin, shown as step 2, thereby reducing congestion.

6. The insertion of a buffer in one segment of a branching connection can increase the speed of the connection on that branch. The speed increases because the inserted buffer reduces the capacitance "seen" by cell 3. That is, cell 3 must drive, or power, several circuit branches before the output signal from cell 3 makes it to the input of cells 4, 10, and 11. The more cells that cell 3 must drive, the slower that portion of the circuit will operate. A typically analogy used in teaching this concept is that a single water faucet will fill one hose much faster than it will fill up several hoses in parallel. In

this analogy, the water is analogous to the signals and the hoses are analogous to the connections between the cells.

7. It is my opinion that at the time the '508 patent was filed in 1998, a person of ordinary skill in the field of Electronic Design Automation (EDA) technology as described in the '508 patent would have had either a Bachelor of Science degree in electrical or computer engineering and approximately five years of experience in the field of EDA software, a Masters of Science degree in electrical or computer engineering and approximately two to three years of experience in the field of EDA software, or a Ph.D. in electrical or computer engineering with a concentration in the field of EDA software.

8. I have studied the claims of the '508 patent, and in my opinion, a person having ordinary skill in the pertinent art in 1998 would interpret the term "bins" in the claims as requiring more than one bin. It is further my opinion that a person having ordinary skill in the pertinent art in 1998 would not have understood the term "bins" as it is used in the '508 patent claims to mean a single bin encompassing an entire integrated circuit chip because the concept of bins was used at that time in connection with partition-based techniques in which the integrated circuit chip was divided into multiple bins. Interpreting the claim term "bins" to mean a single bin is inconsistent with the claim language "selected bins" since to persons skilled in the EDA art, partition-based techniques involved selecting congested bins from among multiple bins; there would be no such selection if only one "bin" existed representing the entire chip.

9. It is further my opinion that all of the logic modifications claimed in '508 patent are performed for the purpose of reducing congestion. The '508 patent is directed to a partition-based technique for improving congestion in an integrated circuit design layout by performing logic modifications. As I noted above, the '508 patent discloses two ways to relieve congestion; a one step process using logic modifications that directly relieve congestion and a two-step process of performing logic modifications to create some timing slack, and then moving the cells to relieve congestion. The logic

modifications performed in both of these processes are done for the purpose of ultimately relieving congestion.

10. Software can execute with a purpose. For example, compression programs have the purpose of compressing files to make them smaller. EDA placement tools execute with the purpose of placing cells onto a chip. Some EDA tools execute with the purpose of improving timing.

11. In Synopsys's Opening Claim Construction brief at page 18 & 19, Synopsys identifies three algorithms corresponding to the claim term "means for performing an initial placement of integrated circuit elements within bins on the design layout" including: (1) "an electronic design automation tool," citing column 3, lines 30-31 of the '508 patent; (2) "a computer executing an algorithm for placing cells in one or more regions using a placement tool that partitions cells into one or more regions at each stage of the placement," citing column 3, lines 31-35 of the '508 patent; and (3) "a computer executing an algorithm for placing cells in accordance with a placement algorithm that is limited by the topology of the circuit" citing column 4, lines 23-29 of the '508 patent. I understand that the parties have agreed that the recited function in the '508 patent claims is "performing an initial placement of integrated circuit elements within bins on the design layout." None of the three portions of the '508 patent referenced by Synopsys disclose a specific algorithm for performing this recited function, and none of these portions of the '508 patent would inform one of ordinary skill in the art that a specific algorithm is being referenced to perform the recited function.

12. The statement in the specification of the '508 patent (column 3, lines 31-35) that "cells are partitioned into a number of bins" may identify the potential result of an algorithm but it does not disclose or inform one of ordinary skill in the art of a specific algorithm that should be used to accomplish that or any other goal. Indeed, there are many different algorithms which could be used to partition cells into a number of bins. Examples include algorithms based on or employing probability distribution functions,

neural networks, functional considerations, timing and congestion and performance, circuit and system hierarchy, simulated annealing, and various genetic algorithms.

13. The statement in the specification of the '508 patent (column 4, lines 23-25) that placement algorithms "are limited in how they can place cells by the topology of the circuit" also does not disclose a specific algorithm or inform one of ordinary skill in the art of a specific algorithm. Rather, it acknowledges an inherent feature of many placement algorithms, namely, that they are constrained by circuit topology.

14. In Synopsys's Opening Claim Construction brief at page 22, Synopsys identifies an algorithm corresponding to the claim term "means for calculating congestion of the initial placement" as being an "interconnection model" citing column 3, lines 35-38 of the '508 patent. I understand that the parties have agreed that the recited function in the '508 patent claims is "calculating congestion of the initial placement." The mention in the specification of the '508 patent (column 3, lines 35-38) of "interconnection models" also does not disclose a specific algorithm or inform one of ordinary skill in the art of a specific algorithm for performing the recited function. Such models, however, may employ many different algorithms, including for example statistic based algorithms, predictive based algorithms, and performance based algorithms.

I declare under penalty of perjury that the foregoing is true and correct.

DATED: November 17, 2006

EDMOND S. COOLEY

CERTIFICATE OF SERVICE

I hereby certify that on November 17, 2006, I electronically filed with the Clerk of Court the **Declaration of Edmond S. Cooley, D. Eng.** using CM/ECF which will send electronic notification of such filing(s) to the following Delaware counsel. In addition, the filing will also be sent via hand delivery:

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I hereby certify that on November 17, 2006, I have sent by electronic mail and First Class Mail, the document(s) to the following non-registered participants:

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